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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,356	04/20/2004	Richard Carl Phelps	0120-027	2594
42015	7590	03/15/2007	EXAMINER	
POTOMAC PATENT GROUP, PLLC			CLEARY, THOMAS J	
P. O. BOX 270			ART UNIT	PAPER NUMBER
FREDERICKSBURG, VA 22404			2111	
SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE		
3 MONTHS	03/15/2007	PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/827,356	PHELPS ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 28 January 2007.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-4 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-4 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____. _____	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 2, and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 4,419,724 to Branigin et al. ("Branigin") and US Patent Number 5,649,159 to Le et al. ("Le").

3. In reference to Claim 1, Branigin discloses an apparatus for use in a computer system comprising: a bus architecture (See Figure 1); a plurality of modules connected to the bus architecture (See Figure 1), each module being assigned an ID (See Column 4 Lines 1-4); each module comprising: reception means for receiving and storing availability data indicative of the availability of modules (See Column 5 Lines 17-22); transaction request means for producing a transaction request including target address data indicating a destination ID for the transaction (See Column 8 Lines 23-29); decoding means for decoding the destination ID to produce an expected destination ID relating to a target module (See Column 8 Lines 27-29); comparison means for

analysing the stored availability data corresponding to the target module identified by the expected destination ID (See Column 8 Lines 29-40); and transaction means, responsive to the comparison means, for terminating the transaction request if the analysed availability data indicates that the target module is unavailable (See Column 8 Lines 29-40). Branigin further discloses the use of device IDs as opposed to memory-mapped devices. Memory mapping devices is a well-known alternative to using device IDs, as evidenced by Le. Branigin does not disclose the target module having an address range in the memory map which includes the target address data; and wherein, for a transaction between an initiating module and a target module, decoding of the target address is carried out in the decoding means located in said initiating module. Le discloses the use of memory-mapped devices in which a target module will have an address range in the memory map which includes a target address data (See Column 2 Lines 17-21 and 43-65); and wherein decoding of the target address is carried out in the decoding means located in said initiating module (See Column 1 Line 65 – Column 2 Line 7, Column 2 Lines 15-27, and Column 4 Lines 20-36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the system of Branigin using the memory mapping of Le instead of device ID's, resulting in the invention of Claim 1, because memory mapping devices is well known, and flexibility can be provided in an integrated circuit unit while constraining the size and complexity of the unit (See Column 2 Lines 22-40 and Column 4 Lines 20-23 of Le).

4. In reference to Claim 2, Branigin and Le disclose the limitations as applied to Claim 1 above. Branigin further discloses a control means for controlling access to the bus architecture by the modules (See Figure 1 Number 100) and wherein the transaction means is further operable to forward, to the control means, a transaction request, if the analysed availability data indicates that the target module is available (See Column 8 Lines 33-40).

5. In reference to Claim 3, Branigin and Le disclose the limitations as applied to Claim 1 above. Branigin further discloses a computer system comprising the apparatus (See Figure 1).

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Branigin and Le as applied to Claim 1 above, and further in view of US Patent Number 5,761,516 to Rostoker et al.

7. In reference to Claim 4, Branigin and Le disclose the limitations as applied to Claim 1 above. Branigin and Le do not disclose an integrated circuit comprising the apparatus. Rostoker discloses an integrated circuit having a plurality of devices, which can include processors, memory controllers, and I/O controllers (See Figure 2 and Column 2 Lines 10-16).

It would have been obvious to construct the device of Branigin and Le on the integrated circuit of Rostoker, resulting in the invention of Claim 4, in order to provide a

more cost-effective use of silicon real estate and provide much better price performance than conventional multichip designs (See Column 1 Line 65 – Column 2 Line 9 of Rostoker).

Response to Arguments

8. Applicant's arguments filed 28 January 2007 with respect to Claims 1-4 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-3), Alt. Fridays (7-2).

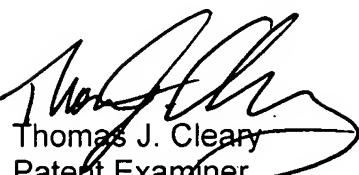
If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TJC



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